# Project description:

## Background

### State of the art:

One of the hottest topics in condensed matter physics is the realization of a quantum computer. The main advantage of such a quantum computer would be its ability to solve specific classes of algorithms orders of magnitudes faster than classical computers. A classical computer is based on deterministic two level states called bits. A quantum computer is also based on two level states (basis states) called quantum bits (qubits). However, a qubit unlike a classical bit exploits the quantum effect of superposition. As a consequence, a quantum system can be simultaneously in both basis states.

There have been several proposals for implementing such a qubit, with just some solid state realizations listed below:

* Electrons on Helium (He) [1]
* Semiconductors:
  + - Nuclear spin qubits [2]
    - Electron (hole) spin qubits [3]
* Superconductors:
  + - Flux qubits [4]
    - Charge qubits [5]

One of the above mentioned suggestions, which came in 1998 by Loss and DiVincenzo, was to use the spin of electrons (holes) for the realization of qubits. The spin, an intrinsic quantum mechanical property of every elementary particle, lifts the degeneracy of an orbital energy level in the presence of an external magnetic field. The orbital level splits into two, typically labelled as spin-up and spin-down. This two level system can then act as a qubit, the so-called spin qubit.

However, for creating and manipulating the spin qubit one must first confine the charge into a region, which is in size comparable to the charge particle wavelength. Such a confinement can take place in a so-called quantum dot (QD). QDs are very small structures (their diameters can reach tens of nanometers) and because of their almost zero dimensionality, the energy levels for a charge particle are discrete and far away from each other.

Not every two level system can create a useful qubit for the realization of a scalable quantum computer. In 1998.. DiVincenzo published a list of conditions which a qubit should fulfill for a quantum computer to work correctly [7]:

The 5 necessary criteria are:

* **The qubit should be well-defined:** A well defined qubit is a two level (two state) system whose levels are distinguishable and highly controllable.
* **It should allow reliable state preparation:** The qubits needs to be deterministically driven into the initial state so that the next computational step can take place**.**
* **It should show low decoherence times (long coherence times):** Because of the several noise sources to which the qubit is exposed its initially prepared state is lost (it does decohere) with time. It is desirable to have as long as possible coherence times.
* **A “universal” set of quantum gates (state manipulation) should exist:** In the classical logic the Boolean function set (set of gates) is functionally complete or universal if any other function (gate) can be represented by it. The same functional universality applies for the quantum logic. *(I think I can say it like this, but I did not find it directly said like that anywhere)*
* **A qubit measurement capability (state readout) should exist:** After a several state manipulations have been applied to the qubit, one should be able to read the computed result, it’s quantum state.

**For all type of qubits there is battle between the manipulation time on one side and the coherence time on the other side. This is so because performing quantum computation, many single operation need to be done before system decoheres. The benchmark for the manipulation time is the minimum time needed for going from the one state to the other.**

**For the spin qubits, which this proposal deals with, different materials have been investigated aiming to find the material with the highest coherence vs manipulation time ratio.**

**Materials**

Silicon **(Si)** has emerged as a promising material for the realization of spin qubits because it can be isotopically purified and left just with the 28Si isotope which is a zero nuclear spin element. Thus the nuclear noise can be eliminated and the coherence time boosted in comparison to the broadly used gallium arsenide (GaAs). The additional big advantage is its compatibility with current CMOS technology. This could become very important when moving towards the realization of a large number of qubits as required by quantum algorithms.

There are several approaches of defining quantum dots (QDs) in silicon.

One way is by means of a phosphorous (P) dopant. In that case a P atom behaves as an electron quantum dot because of its confining potential. Andrea Morello’s Group from the UNSW in Australia, by applying the Hahn echo pulse sequence, has measured electron spin coherence time T2ECHO exceeding 200 microseconds, in a non – isotopically purified Si:P system, while the duration of one full spin rotation in this case is τπ = 75 ns [3]. By using isotopically purified 28Si:P samples and the nuclear spin of an P atom as a qubit, the same group has achieved nuclear spin coherence time of 60 milliseconds using spin-echo technique and duration of the π rotation approximately τπ = 50 μs [2].

M. Veldhorst et al. by using lithographically defined electron QDs in Si have measured spin coherence times using the CPMG pulsing technique of T2CPMG = 28 ms and τπ = 1.5 μs [17].

Finally, E. Kawakami et al. by using a single-electron QD in a Si/SiGe heterostructure qubit, have measured T2ECHO = 40 μs, while τπ = 0.15 μs [18].

One limitation of Si is the difficulty to perform fast gate operations while maintaining the good coherence. One way around this problem is to use the spin-orbit interaction of holes and perform spin manipulation via electric fields (as described in more detail in the *Spin manipulation measurements* section). Using this approach R. Maurand et al., realized very recently the first CMOS spin qubit by using a hole confined in a transistor made out of p-type Si. The reported T2ECHO time was 245ns for a π spin rotation time of approximately τπ = 3 ns. [11].

Holes in germanium (**Ge)**, on the other hand, have much higher spin orbit coupling which should allow much **faster spin manipulation times**. In addition, for purely heavy-hole (HH) states the dephasing time should be very long [21].

In our group we study qubits, in Ge self-assembled nanostructures [10], which are created by epitaxial growth of Ge on Si. Such a growth can lead to various types of nanostructures. In this project the so-called Ge hut-wires are going to be studied. Very recently magnetotransport measurement have shown that holes, in this type of structures, are of the HH character, suggesting long coherence times for this material system.

**C:\Users\jkukucka\Documents\GitHub\Fellowship\Diamond_Hannes.tif**

Figure 1: Stability diagram of a SiGe nanowire single quantum dot (left). Scanning electron micrograph of SiGe nanowire contacted by palladium Pd source and drain electrodes (right) [10]

**Measurement techniques:**

Different type of measurement techniques have been used in order to extract the state of a spin qubit and its coherence time:

* DC current readout: The DC current readout is sensing the electron transport through the qubit by means of current measurement. It is prone to low frequency 1/f noise and the bandwidth (BW) is low because of heavy filtering necessary for achieving low effective electron temperatures.
* Differential measurement (AC current readout): The differential measurement (AC current readout) has the same drawbacks as DC current readout. It is typically done with a low frequency lock in technique. Because of the low frequency noise, a lock in amplifier usually operates on a very narrow BW around the measurement frequency, which leads to long measurement times (let’s discuss this).
* Ohmic reflectometry: Ohmic reflectometry is a technique which indirectly senses the impedance change of a QD by monitoring the amplitude or phase of the reflected from the QD wave (see Figure 3 for a more detailed explanation). It is usually performed by high frequency lock-in techniques and is not prone to 1/f noise.
* Gate reflectometry: Similar to the ohmic reflectometry but it is connected to a gate and not to the source or the drain lead. **It’s big advantage is that it does neither require charge transport through the QD hosting the qubit nor the existence of a charge sensor.**

**Explanatory box: What is reflectometry?**

****

Figure 3: Basic principle of ohmic reflectometry. The Resonant circuit is consisting of the SHT sample and matching circuit. SHT sample is represented with parallel combination of CS and RS. S and D denote the source and drain contacts of the SHT, respectively. The matching circuit formed with an inductor L and a capacitance C is connected to the source contact.

Reflectometry is a readout technique based on the change of the wave reflection coefficient Γ. It comes from the electromagnetic wave principle – if a wave is travelling in a media with impedance Z0  (e.g. coaxial cable) and it encounters a change of impedance from Z0 to Z (e.g. end of coaxial cable), a portion of the wave will be reflected back according to the expression: , where Ar is the amplitude of the reflected signal, Ain the amplitude of the incoming wave and Γ is the reflection coefficient.

By using a resonant circuit (matching circuit with an incorporated SHT) as showed in Figure 3, instead of the open end of a coaxial cable one can make use of the information contained in the reflected wave amplitude. For achieving this, the elements of the resonant circuit, the inductance L and the capacitance C needs to be chosen to achieve the matching condition on the resonant frequency of the circuit, . Matching condition is the situation in which the typically large resistance (~100 KΩ) of the SHT is transformed, by the inductor and capacitor, to near 50 Ω. This value is the characteristic impedance of the RF line Z0, thus the wave reflection coefficient Γ is minimized. In that case sensitivity is maximized [13] and small changes in the SHT impedance results in an observable change in the reflected wave amplitude.

Thus, if a hole tunnels -> SHT impedance changes -> Γ changes -> amplitude and phase of the reflected wave changes.

### Definition of the problem:

**Since charge transport through the QD hosting the qubit, is in many qubit experiments unwanted because it is an invasive method, alternative methods have been looked for.** A usual solution to this problem is to place, next to a measured qubit, an additional, separated QD in the form of a single electron (hole) transistor or a quantum point contact, called charge sensor. The charge sensor is electrostatically coupled and thus sensitive to the charge configuration in the qubit. The charge sensor itself is well coupled to ohmic contacts thus it is suitable for charge transport measurements (DC current readout, AC current readout) and ohmic reflectometry.

**However, charge sensors suffer from thermal broadening of the conductance features (coulomb peaks, conductance plateaus) which lowers the sensitivity and thus the readout speed. In addition, their gate voltage needs also to be continuously adapted in order to compensate the influence of the qubit gates on their conductance. Finally, by looking into the future, for the realization of a usable quantum processor, the qubit number needs to be drastically scaled up. Adding charge sensors next to each qubit will lead to additional complexity.**

**Gate reflectometry does not suffer from the previously listed problems.**

By connecting the gate electrodes defined for creating and tuning a DQD in GaAs/AlGaAs heterostrucure to a lumped element resonator acting as a gate reflectometry circuit, J. I. Colless et al. achieved a charge sensitivity of 6.3 meHz-1/2 (smaller is better) [14]. Last year, M.F. Gonzalez – Zalba et al. reported an improved charge sensitivity of 37 μeHz-1/2 by using the similar gate reflectometry approach for a silicon nanowire based DQD device [12]. The reported sensitivity is similar to that achieved with ohmic reflectometry in charge sensors such as 1 μeHz-1/2 for RF quantum point contact and 100 μeHz-1/2 for RF single electron transistor [12].

High sensitivity and thus high speed of the gate reflectometry circuit is desired for performing spin state measurements in the single shot regime. Also it is desired for capturing fast stability diagrams (which usually can take up to several hours using DC or AC current readout techniques) and thus performing the measurements much faster

### Proposal objectives:

The objectives of this proposal are to **design a** **fast gate reflectometry** system which will be used in order to study in second part of my PhD thesis the spin properties of the Loss-DiVincenzo qubit created in a Ge- based, double quantum dot.

For the gate reflectometry, the goal is to achieve a charge sensitivity comparable or even faster than the one reported in [12]. That will allow us to have a high bandwidth system necessary for the qubit read out. After the gate reflectometry will have been set up the focus will go to the realization of the Loss-DiVincenzo hole qubit in a DQD structure. The first measurements to be performed are the ones for determining the spin relaxation time T1 . Subsequently experiments in order to investigate the coherence time of the qubit are going to be performed. More concretely, spin manipulation experiments for measuring the spin dephasing time T2\*, the spin coherence time using Hahn echo technique T2ECHO, and the spin coherence time using the CPMG (Carr-Purcell-Meiboom-Gill) pulse sequence technique T2CPMG, are going to be conducted.

### Working schedule:

#### Designing initial version of reflectometry setup: sample holder, readout circuit, instrumentation setup

**Sample holder**

In order to tune the gate reflectometry system, measurements will be initially performed at 4K, by using a single QD device as SHT. During the first year of my PhD I have already prepared a 4K dip stick (Figure 4) for such reflectometry measurements. Particular attention was paid to the sample holder, fabricated out of a printed circuit board (PCB). DC electrical signals are sent to the sample through low thermal conductive wires twisted in pairs finishing in a PCB connector; radio frequency (RF) signals are sent through the coaxial cables. The DC signals are low pass filtered with surface mounted RC filters (Figure 5) to reduce thermal noise from the wires. After low pass filtering, the DC signals are routed to the gold plated bonding pads around the area in the middle of the PCB (sample area) on which a typically 5x5 mm sample is glued with silver paste (Figure 5). The RF coaxial lines are finishing on the PCB mounted SMP connectors. After the SMP connector, a DC signal is added to the RF signal by using a bias tee. From there the signal is routed to the PCB bonding pads. Electrical contacts from the PCB bonding pads to the sample bonding pads are achieved by wedge wire bonding.

**

Figure 4: Plexiglas 4K dip-stick used for cooling down samples to 4K and performing reflectometry measurements. The left picture shows the whole stick, while the right is a zoom-in, highlighting the directional coupler and the low noise Minicircuits ZX60-33LN-S+ RF amplifier. An additional low noise cryogenic RF amplifier CITLF2 from Sander Weinreb’s Caltech Microwave Research Group can be added in order to increase the SNR of the measured signal.

****

****

Figure 5: Initial version of the PCB sample holder. The left figure show the upper view of the PCB board while the right figure focuses on the back side.

**Resonant Circuit**

The used resonance circuit consisted of a matching circuit (Figure 5) and the SHT. SHT is schematically presented as resistance RS in parallel to the capacitance CS, as can be seen in a simple circuit model in Figure 3. For the matching circuit, the surface mounted inductor Murata 1.2 μH and the varactor MACOM MA46H070-1056 were used. The Varactor – a voltage tunable capacitor - was used in order to be able to always achieve a good matching condition despite the change of the SHT resistance Rs [13], as explained in “What is reflectometry” section of the “State of the art” chapter.

For performing the ohmic reflectometry measurements the RF signal was sent down the coax line (Figure 4, right) towards the QD device. The signal which gets reflected from the resonant circuit is sent via the directional coupler to the amplifiers. The amplifier configuration, shown in Figure 4 (right), is used to preserve the signal to noise ratio (SNR). After the sample, a very low noise cryogenic amplifier, Weinreb’s CITLF2, is used to amplify both signal and noise by the same amount (around 20 dB), adding a very small amount of itself noise, thus almost equalizing the SNR on its input with SNR on its output. Higher noise level on the output of the CITLF2 amplifier allows the second, noisier amplifier to achieve SNR on its output approximately same as the SNR on its input. Such an amplifier chain enables non – degrading propagation of the SNR from the sample stage to the higher noise room temperature electronics [is the critical characteristic the input noise or the output noise of the amplifier? Question not necessary important for the proposal ☺] .